AMENDMENTS TO THE CLAIMS

Please amend the claims of this application as follows:

Claims 1-37. (Cancelled).

38. (New) An addressing structure for addressing a display medium, the structure comprising:

a plurality of column electrodes, each of the column electrodes being connected via switch means to a plurality of pixel electrodes;

a plurality of voltage sources each having a different voltage level; and

a switch unit having a plurality of voltage source inputs each connected to one of the plurality of voltage sources, and a plurality of outputs each connected to one of the plurality of column electrodes, the switch unit being capable of connecting each of the column electrodes independently to selected ones of the plurality of voltage sources.

39. (New) An addressing structure according to claim 38 wherein the switch unit further comprises at least one display signal input arranged to receive a display signal specifying the voltages to be placed upon the column electrodes, and the switch unit is arranged to connect each of the column electrodes independently to selected ones of the plurality of voltage sources dependent upon the display signal.

40. (New) An addressing structure according to claim 39 wherein the switch unit comprises one display signal input for each column electrode and the switch unit is arranged to connect each column electrode to a selected one of the plurality of voltage sources dependent upon the display signal received by the display signal input associated with the column electrode.

41. (New) An addressing structure according to claim 39 further comprising a data register for receiving sequentially data representing voltages to be applied to each of the column electrodes, and for storing said data, and data latching means for receiving said data from the data register, the at least one display signal input being connected to the data latching means.

42. (New) An addressing structure according to claim 38 wherein the switch unit comprises a plurality of multiplexing units, one multiplexing unit being connected to each column electrode, each multiplexing unit comprising a number of switches equal to the number of voltage sources inputs of the switch unit, each switch being capable of connecting its associated column electrode to its associated voltage source input, the multiplexing units being arranged to that, in each multiplexing unit only one of the switches is closed at any given time, all the other switches being open.

43. (New) An addressing structure according to claim 38 wherein the switch unit further comprises a blanking signal input arranged to receive a blanking signal, the switch unit being arranged to that, upon receipt of the blanking signal, all column electrodes are connected to the same voltage source.

44. (New) An addressing structure according to claim 38 wherein the switch unit comprises a primary switch unit, a plurality of voltage rails, a plurality of secondary switch units each having an output connected to one column electrode, and sequencing means, the primary switch unit having voltage source inputs connected to the voltage source inputs of the switch unit, voltage rail outputs each connected to one voltage rail, and at least one control signal input arranged to receive a primary switch unit control signal from the sequencing means, each secondary switch unit having voltage rail inputs connected to each of the voltage rails and a control signal input arranged to receive a secondary switch unit control signal from the sequencing means, the sequencing means controlling the primary switch unit so that the voltage rails are connected to a first subset of the voltage source inputs of the primary switch unit during a first period, and to a second subset, different from said first subset, of the voltage source inputs of the primary switch unit during a second period, and each of the secondary switch units being arranged to connect their associated column electrode to a selected one of the voltage rails dependent upon the secondary switch unit control signal.

45. (New) An addressing structure according to claim 44 wherein one voltage rail is maintained at the same voltage during the first and second periods.

46. (New) An addressing structure according to claim 45 having at least three voltage rails, a first voltage rail maintained at the same voltage during the first and second periods, a second voltage rail maintained positive with respect to the first voltage rail during the first and second periods, and a third voltage rail maintained negative with respect to the first voltage rail during the first and second periods.

47. (New) An addressing structure according to claim 44 wherein the sequencing means is arranged to receive a digital display signal comprising a plurality of digits defining the voltages to be applied to a given column electrode, and the sequencing means controls the secondary switch units such that the signal applied to that column electrode during the first period is defined by one digit of the digital display signal and the signal applied to that column electrode during the second period is defined by a second digit of the digital display signal.

48. (New) An addressing structure according to claim 44 wherein the voltage sources comprise a voltage source having a central voltage at which the voltage rail is maintained during the first and second periods, a predetermined number of voltages greater than the central voltage and the same predetermined number of voltages less than the central voltage.

49. (New) An addressing structure according to claim 48 wherein the differences between the central voltage and the predetermined number of voltages greater than the central voltage form a geometric series 1, 2, 4 etc. and the differences between the central voltage and the predetermined number of voltages less than the central voltage form a similar geometric series.

50. (New) An electro-optic display comprising:

a transparent substrate bearing a single transparent common electrode;

an addressing structure according to claim 38; and

an electro-optic medium disposed between the pixel electrodes of the addressing structure and the common electrode, the common electrode extending across all the pixels of the display.

51. (New) An electro-optic display according to claim 50 wherein the switch unit of the addressing structure comprises a blanking signal input arranged to receive a blanking signal, the switch unit being arranged to that, upon receipt of the blanking signal, all column electrodes are placed at the same voltage as the common electrode.

52. (New) An electro-optic display according to claim 50 wherein the switch unit of the addressing structure comprises a primary switch unit, a plurality of voltage rails, a plurality of secondary switch units each having an output connected to one column electrode, and sequencing means, the primary switch unit having voltage source inputs connected to the voltage source inputs of the switch unit, voltage rail outputs each connected to one voltage rail, and at least one control signal input arranged to receive a primary switch unit control signal from the sequencing means, each secondary switch unit having voltage rail inputs connected to each of the voltage rails and a control signal input arranged to receive a secondary switch unit control signal from the sequencing means, the sequencing means controlling the primary switch unit so that the voltage rails are connected to a first subset of the voltage source inputs of the primary switch unit during a first period, and to a second subset, different from said first subset, of the voltage source inputs of the primary switch unit during a second period, and each of the secondary switch units being arranged to connect their associated column electrode to a selected one of the voltage rails dependent upon the secondary switch unit control signal, and wherein one voltage rail is maintained at the same voltage as the common electrode during the first and second periods.

53. (New) A method for addressing a display medium, the method comprising:

providing a plurality of voltage sources each having a different voltage level;

providing a plurality of column electrodes, each of the column electrodes being connected via switch means to a plurality of pixel electrodes, the pixel electrodes being arranged to apply electric fields to pixels of the display medium;

providing a switch unit having a plurality of voltage source inputs each connected to one of the plurality of voltage sources, and a plurality of outputs each connected to one of the plurality of column electrodes, the switch unit further comprising a display signal input arranged to receive a display signal,

by means of the switch unit, connecting each of the column electrodes independently to selected ones of the voltage sources, the voltage source connected to each column electrode being controlled by the display signal.

54. (New) A method according to claim 53 comprising receiving in a data register data representing the voltages to be applied to each of the column electrodes, storing said data in said data register, transferring said data to a data latching means, and generating the display signal dependent upon the data in the data latching means.

55. (New) A method according to claim 53 wherein the switch unit further comprises a blanking signal input, and the method further comprises supplying a blanking signal to blanking signal input and thereby causing the switch unit to connect all the column electrodes to the same voltage source.

56. (New) A method according to claim 53 wherein the switch unit comprises a primary switch unit, a plurality of voltage rails, a plurality of secondary switch units each having an output connected to one column electrode, and sequencing means, the primary switch unit having voltage source inputs connected to the voltage source inputs of the switch unit, voltage rail outputs each connected to one voltage rail, and at least one control signal input arranged to receive a primary switch unit control signal from the sequencing means, each secondary switch unit having voltage rail inputs connected to each of the voltage rails and a control signal input arranged to receive a secondary switch unit control signal from the sequencing means,

the method comprising (a) during a first period, sending a first signal from the sequencing means to the primary switch unit so that the voltage rails are connected to a first subset of the voltage source inputs of the primary switch unit, and during the same first period sending second signals from , and to a second subset, different from said first subset, of the voltage source inputs of the primary switch unit during a second period, and each of the secondary switch units being arranged to connect their associated column electrode to a selected one of the voltage rails dependent upon the secondary switch unit control signal.

57. (New) A method for addressing a display medium, the method comprising:

providing a first column electrode, a first pixel electrode, a first capacitor connected to the first pixel electrode, and a first resistive switch means having an open position in which the first column electrode is not connected to the first pixel electrode, and a closed position in which the first column electrode is connected via a resistance to the first pixel electrode;

providing a second column electrode, a second pixel electrode, a second capacitor connected to the second pixel electrode, and a second resistive switch means having an open position in which the second column electrode is not connected to the second pixel electrode, and a closed position in which the second column electrode is connected via a resistance to the second pixel electrode;

placing both the first and second switch means in their closed positions, thereby connecting the first and second column electrodes to the first and second pixel electrodes respectively;

applying a drive voltage to the first column electrode for a first period of time, thereby charging the first capacitor to a first addressing voltage different from the drive voltage; and

applying the drive voltage to the second column electrode for a second period of time, thereby charging the second capacitor to a second addressing voltage different from both the drive voltage and the first addressing voltage.

58. (New) A method according to claim 57 wherein the first and second periods are multiples of a predetermined interval.

59. (New) An addressing structure for addressing a display medium, the structure comprising:

a first column electrode, a first pixel electrode, a first capacitor connected to the first pixel electrode, and a first resistive switch means having an open position in which the first column electrode is not connected to the first pixel electrode, and a closed position in which the first column electrode is connected via a resistance to the first pixel electrode;

a second column electrode, a second pixel electrode, a second capacitor connected to the second pixel electrode, and a second resistive switch means having an open position in which the second column electrode is not connected to the second pixel electrode, and a closed position in which the second column electrode is connected via a resistance to the second pixel electrode;

switch control means arranged to move the first and second switch means to their closed positions; and

voltage supply means arranged to place a driving voltage on the first and second column electrodes while the first and second switch means are in their closed positions, the voltage supply means being capable of applying the drive voltage to the first column electrode for a first period and of applying the drive voltage to the second column electrode for a second period different from the first period.

60. (New) An addressing structure according to claim 59 wherein the first and second periods are multiples of a predetermined interval.